**ELEC 204 Digital Design Preliminary Lab Report**

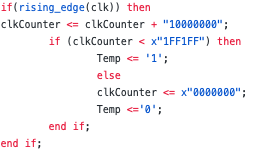
Preliminary Lab 4

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**Question 1**

In previous lab. We used slower Clock which is in Figure 1. This decreases clock frequency around 48 Hz. So, this cannot be seen by our eyes. We can change the clock speed of the 7-segment display to a speed in which the multiplexing of the seven segment is visible. If I increase counter “1FF1FF” we can’t see multiplexing of the 7-segment clearly because our eyes can’t differ above 26 Hz. That’s why if I increase this number multiplexing over Leds will change slower. (I use numbers method to light Leds. From leftmost bit to right most bit in seven segment driver modules.)



**Figure 1.** 7-segment Clock divider

**Question2**

For a 100 MHZ master clock and a desired 1Hz clock what is the number we need to reset the counter in (N in the clock divider section)?

100MHz is equal to 108 Hz, so to set slower clock frequency we need to count until 108. That’s why I used property of VHDL to see easily. I have written my code with integer. Also, we can do it with binary code.

ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure 2.** clock for 1 HZ(1 sec)

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Açıklama otomatik olarak oluşturuldu

**Figure 3.** clock divider for 1 Hz with Binary



**Figure 3.** clock for 100Hz(1/100 second used in chronometer)

mathematical relation between the Master clock frequency (FM), Slower clock frequency (FD) and N can be seen on left figure.

In this lab instead of giving clock for each clock elements (second\_clock, minute\_clock, hour\_clock, millisecond\_clock). I used one clock then I deal with in debouncing module. You can check my code for how to handle that with one clock.

FM = 100MHz, Fd = 1 Hz

(FM)= (Fd)\* N

tFd = 1 s (for Fd that we needed) so,

tFm = 1/100 Mhz = 1/ 8\*108 Hz = 10-8 s

1/(10-8s) = 1/(1s) \* N => N = 108

**Question 3.**

(the number of bits needed for the N of the question 4.2.) According to mathematical relation we need counter until decimal integer: 108. This number is base 10 so if we translate into binary, we can see how many bits are needed for clock divider.

(108 )10 = (5F5E100)16 = (0101111101011110000100000000)2

So we need 28 bits to count up to 108.(converting to the BCD 28 bits needed)